Thermal and Electrical Instability of Amorphous Silicon Thin-Film-Transistor for AM-FPD's

Alex Kuo and Jerzy Kanicki

Organic and Molecular Electronics Laboratory
Solid State Electronics Laboratory
Department of Electrical Engineering and Computer Science,
The University of Michigan, Ann Arbor, Michigan 48109, USA
Phone: +1-734-936-0972 Fax: +1-734-615-2843 E-mail: kanicki@eecs.umich.edu

We report on the thermal and electrical instability of hydrogenated amorphous silicon thin-film-transistors (a-Si:H TFT) that are relevant to active-matrix flat panel displays (AM-FPD's). Bias temperature stress experiments were performed on the TFT's, and we concluded that their optimum operating regime with minimum degradation ocurred in the saturation regime. The TFT current temperature stress experiments were also conducted in order to quantify the device degradation under different stress currents. Both device stress data must be considered separately for a given AM-FPD application.

1. Introduction

Amorphous silicon TFT has been a desirable choice in flat panel display technology for more than two decades. It is important to have a thorough understanding on the influence of the bias, current, and temperature on the device aging of the TFT if we want to extend its application to future AM-FPD. It is known that the degradation of the a-Si:H TFT performance can negatively impact the viewing quality[1,2]. In this study, we extract a-Si TFT's electrical parameters at high temperature, and evaluate the device's instability due to electrical, both bias and current, and thermal stressing.

2. Experimental

The chromium bottom-gate back channel etch a-Si:H TFT's (W/L = 40/13.3) were used in this study[3,4]. The electrical measurements were carried out in a Karl Suss probe station with heated chuck and a Signatone temperature controller. Electrical characteristics were measured using an HP 4156A Parameter Analyzer via an ICS software on a computer.

To investigate the operation of the TFT under different temperature, we measured the linear ($V_{DS}<V_{GS}-V_T$) and saturation ($V_{D\text{-}SAT}\geq V_{GS}-V_T$) regime transfer characteristics of the transistor at temperature ranging from 293 to 423K at intervals of 10K. During the electrical measurement of the TFT operating in the linear regime, the parameter analyzer internally grounded the source terminal, applied a constant voltage of 0.1V on the drain, and swept the voltage on the gate terminal from -10V to 20V with 0.5V interval. For the operation of the TFT in the saturation regime, the setup was identical except the analyzer internally shorted the drain and gate terminals together instead of applying a constant bias on the drain. The currents flowing into the drain, gate, and sources were collected by the system. Throughout the measurement, the substrate remained at a constant temperature, with fluctuation of less than 0.1 ºC. We follow the extraction methods used by *Martin et al*[5] to obtain the field-effect mobility (μ_{EFF}), threshold voltage (V_T), subthreshold swing (S), and gamma factor (γ) from the transfer characteristics based on the following equations:

$$I_{D-LIN} = \frac{W}{L}\mu_{EFF}C_{INS}(V_{GS}-V_T)^{\gamma}V_{DS} \qquad (1)$$

$$I_{D-SAT} = \frac{W}{2L}\mu_{EFF}C_{INS}(V_{GS}-V_T)^{\gamma+1}. \qquad (2)$$

We also measured the TFTs' performance after applying electrical bias and current stress at elevated temperature (353K or 80 ºC). During the bias temperature stress (BTS) experiments, constant biases were applied continuously to the terminals of the TFT's, only stopping to measure the saturation transfer characteristics of the transistors. The transfer characteristics were measured for stressing time (t_{STR}) of 0 to 10000 seconds. Four BTS experiments were carried out with the following biasing conditions: a) V_{GS}=V_{DS}=40V, b) V_{GS}=40V and V_{DS}=0V, c) V_{GS}=40V and the drain was floating, and d) V_{GD}=40V and the source was floating.

During the current temperature stressing (CTS) experiment, constant electrical currents (I_{STR}) flowed into the drains of the TFT's at elevated temperature (80 ºC). The measurement technique and time intervals were the same as the BTS experiments. Three stressing currents were chosen for the experiments: I_{STR}=10nA, 500nA, and 5.5µA. The I_{STR}s' selected reflect the current levels required to drive an OLED pixel of a XGA display. We performed separate CTS experiments on TFT's operating in linear and saturation regimes. In the linear regime, the gate was biased at 20V while I_{STR} flows into the drain of the TFT. In the saturation regime, the gate and the drain were externally shorted together ($V_{DS}(t)$=$V_{GS}(t)$) during the CTS experiments, which meant the I_{STR} flowed into the drain and set up the bias on the gate.

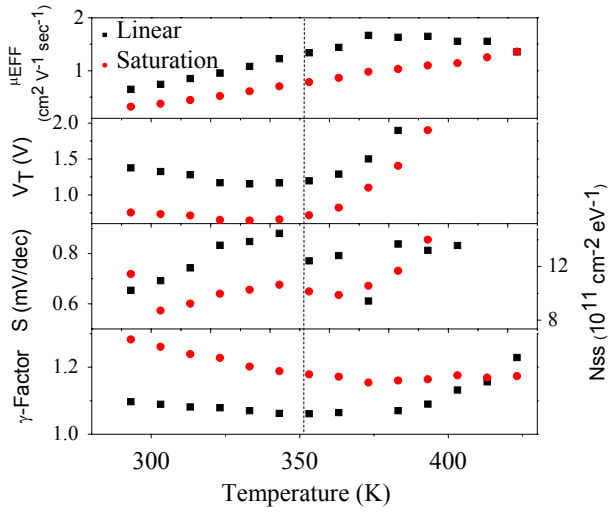

Figure 1: Variations of a-Si:H TFT's μ_{EFF}, V_T, S, and γ with temperatures from 293 to 423K.

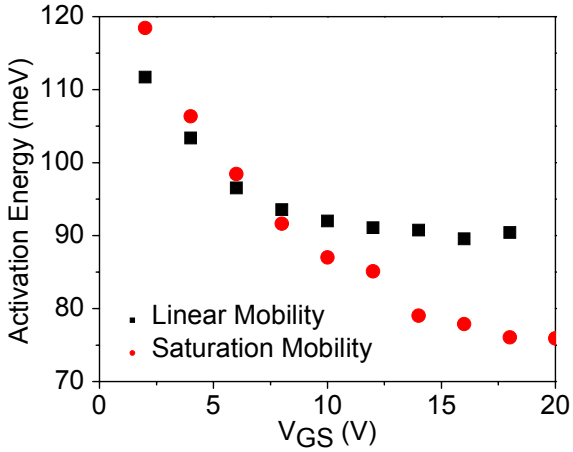

Figure 2: Variation of a-Si:H TFT activation energy with gate bias from V_{GS}=0 to 20V.

3. Results

High Temperature Analysis

Figure 1 shows the extracted μ_{EFF}, V_T, S, and γ of the transistors at different temperatures. Both μ_{EFF} and S increase with temperature, while V_T and γ decrease with increasing temperature. At temperatures above 80ºC, the characteristic of the TFT changes during the electrical measurement, and we can no longer use our conventional methods of extraction to obtain meaningful device parameters. However, we still show the results based on our method of extraction for completeness. We extracted the activation energy at different gate biases following method described by Lustig *et al*[6,7,8] and the resulting activation energies at various gate biases are shown in figure 2, and they vary from 75 to 120meV. The trend and range is consistent with the values report by Lustig *et al*[5]. The increase in the field-effect mobility and decrease in the threshold voltage at higher temperature are very attractive characteristics of a-Si:H TFT for display application.

Bias Temperature Stress

Figure 3 (top) shows the evolution of the transfer characteristics with t_{STR} for BTS condition (a) in linear scale.

The device degradation is defined as the shift in mid-gap voltage (ΔV_{MG}),

$$V[I_{D-SAT}^{1/2}(t=t_{STR})]-V[I_{D-SAT}^{1/2}(t=0)] \quad (3)$$

$$\text{at} \quad I_{D-SAT}^{1/2}=\frac{1}{2}I_{D-SAT}^{1/2}(MAX)].$$

This allows us to indiscriminately quantify the characteristic shift due to applied electrical stress. Figure 4 shows the variations of the ΔV_{MG} for all four BTS conditions described above, in both log and linear scales. The largest degradation (b) occurs when a high electric field (1MV/cm) is setup across the entire gate insulator, assuming the entire channel area is grounded by the source and drain terminals. Conditions (c) and (d) have similar ΔV_{MG} compared to condition (b) up until t_{STR}=1000sec, and decrease beyond that point. Since either the drain or the source is floating in each condition, the electric field across the insulator near the electrically floating region has to be equal to or lower than 1MV/cm. The lowest shift occurs in condition (a), even though it has the highest drain current during the electrical stressing. This suggests that high electric-field-induced trapping across the nitride is responsible for the device characteristic shift[9,10]. Moreover, the result indicates that the most stable operational regime for a TFT is in saturation because the gate electric field near the drain region is minimized.

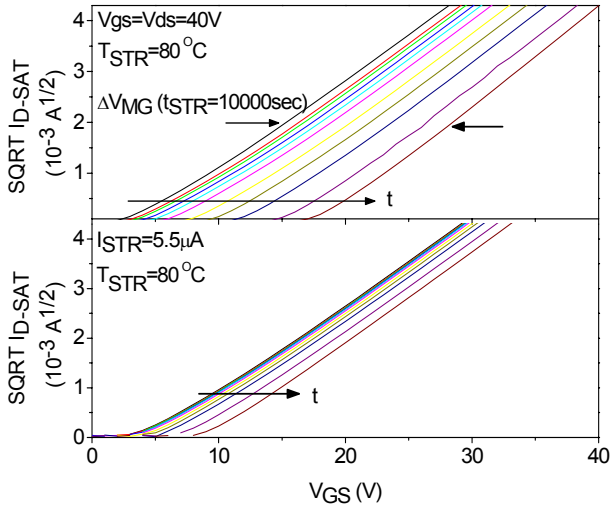

Figure 3: Variation of the saturation regime TFT transfer characteristic during BTS (top) and CTS (bottom) for t_{STR}=0 to 10000sec.

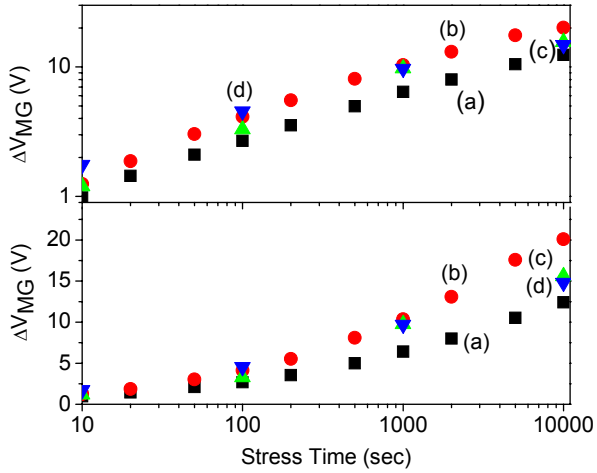

Figure 4: Variation of ΔV_{MG} for the following BTS conditions: a) V_{GS}=V_{DS}=40V, b) V_{GS}=40V and V_{DS}=0V, c) V_{GS}=40V and the drain is floating, and d) V_{GD}=40V and the source is floating.

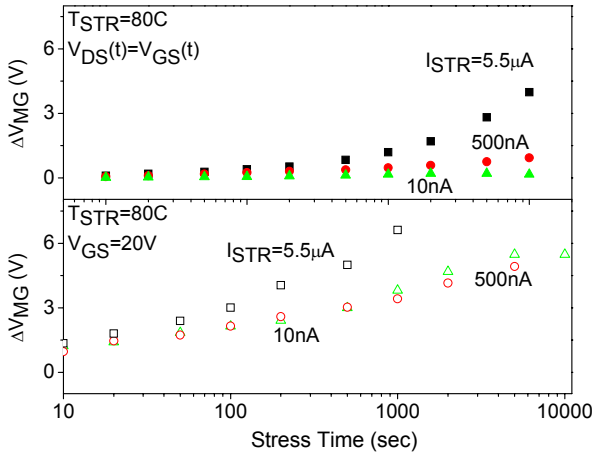

Figure 5: CTS ΔV_{MG} for V_{GS}(t)= V_{DS}(t) (top) and V_{GS}=20V (bottom).

Current Temperature Stress

The extraction of device degradation for CTS is exactly the same as for BTS, and the TFT transfer characteristics for different t_{STR} are shown in figure 3 (bottom). The ΔV_{MG}

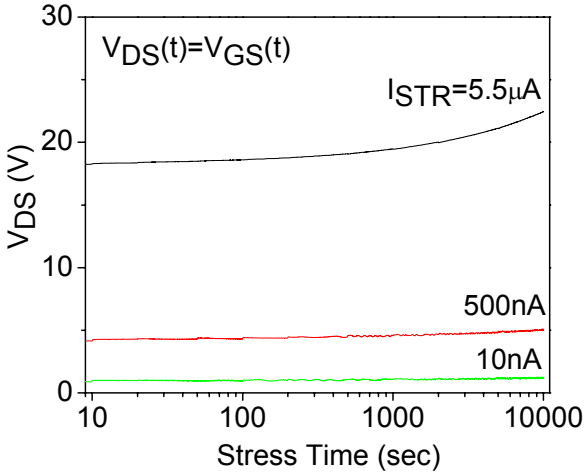

Figure 6: Drain voltage versus stress time for saturation regime CTS.

plot versus t_{STR} of the TFT's under CTS is shown in figure 5. The top portion represents the CTS experiments conducted under saturation regime of operation and the bottom portion represents the linear regime of operation. The TFT's undergoing current temperature stress suffer larger device degradation when they operate in the linear regime than the saturation regime. The result is consistent with the BTS experiments. In both linear and saturation regimes CTS, the drain voltage increases with t_{STR} to maintain the current level flowing through the TFT. Figure 6 shows the drain voltage versus stress time for saturation regime CTS; the increase in V_{DS} is the largest for I_{STR}=5.5μA because it has the highest ΔV_{MG}.

4. Conclusion

We studied the electrical behavior of a-Si TFT at elevated temperature. Above 80ºC the transistor becomes electrically unstable, thus becomes difficult to extract its true device parameters. Bias temperature stress and current temperature stress experiments were conducted to evaluate the stability of the device under prolong voltage and current stress, respectively. A TFT can undergo characteristic shift even if there is no drain current flowing, but a positive bias is applied on the gate. Since both drain current and electric field across the gate insulator contribute to device degradation, the most stable condition to operate a TFT is in saturation regime, when the electric field across the gate insulator is minimized. Hence, to improve the stability of a thin film transistor we need to either increase its mobility, gate insulator capacitance, or the W/L ratio. Finally it is critical to operate a-Si:H TFT in AM-FPD at the optimum operating temperature if we seek to balance its device electrical performance and instability.

Acknowledgement

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